Dual-V_{DD} Pass Transistor Logic for Reduced Delay in Low-Power Operation

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Project Proposal

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Problem

As transistor sizes have continually scaled down, leakage current has contributed more and more to overall energy consumption, motivating research into leakage reduction techniques, including sub-threshold operation for ultra-low power applications. One potentially interesting technique is the use of pass-transistor logic (PTL), in which transistors are interconnected only by their source-drain terminals rather than leaving direct leakage paths through pull-up and pull-down networks positioned between the supply rails. This approach can be accomplished with transmission gates, or better yet, with only nMOS transistors for a reduction in area, with the consequence of a reduced output voltage swing, giving rise to increased delay and thus exacerbating the effects of subthreshold operation. However, it has been observed that driving the gate terminals of a PTL network at a higher-than-V_{DD} level can improve this delay. Thus, in order to address the problem of reducing leakage while taking advantage of the area reduction offered by nMOS PTL and yet still limiting the associated increase in delay, we propose the use of dual-V_{DD} rails for separately driving gate and source-drain terminals of a PTL network. Specifically, we examine this approach in context of a lookup table (LUT) for an FPGA basic logic element (BLE).

Related Work

Dual-V_{DD} supplies have been used in previous work, including FPGAs. For example, Li et al. use alternating rows of high- and low-voltage logic blocks in an FPGA fabric [1], while Gayasen et al. allow the supply for each block to be chosen programmatically, such that blocks not in the critical path can run at a lower voltage [2]. Both approaches segment the high- and low-voltage supply zones at the block level. In contrast, Ryan et al. use a dual-V_{DD} scheme whose boundary is at the FPGA interconnect configuration; the interconnect signals are low-swing while the switch blocks consist of passgate transistors driven by high-V_{DD} inputs in static configuration [3]. This approach offers a 14X speed up and 22X reduction in energy in a subthreshold FPGA, a result that holds potential for optimizing the logic blocks themselves at the LUT level.

One problem with typical PTL design is the existence of "sneak paths" for leakage between multiple source-drain-terminal inputs, when one input is at V_{DD} and a nearby input is at GND. Alarcón et al. present an alternate style of PTL targeted for low-leakage operation in above-threshold operation by eliminating these "sneak leakage paths" [4]. Whereas a typical PTL hierarchical mux would consist of a collapsing tree of passgates, the authors use an "inverted tree," or "stack," that fans outward, which has a single source-drain-terminal input at the root, driven by an inverter. This topology, shown in Fig. 1, is configured to implement an arbitrary logic function by connecting each leg's output to one of two differential outputs, S and SB, which are connected to a sense amp. While the circuit is intended

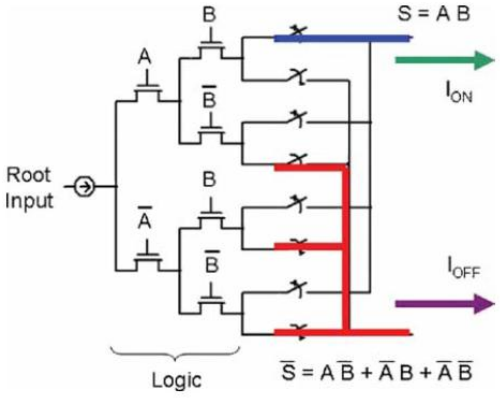

Figure 1. PTL stack topology wired for 2-bit AND. Only either S or SB is driven at a time [4].

for static configuration by fixed wiring at design time, it can be adapted to implement a programmable LUT by replacing the switches pictured with passgate transistors, which are driven by SRAM bit-cells storing the configuration for that LUT. It should be noted that one disadvantage of this topology is a requirement to pre-discharge the entire network before each operation, under control of a clock signal.

Approach

Design

We first need to establish a base case to compare against, which in this case will be a transmission gate mux based LUT. The main design component required for the transmission gate mux will be modifying it to work in sub threshold and with dual-V_{DD} operation.

The first alternative topology we will look at is a standard pass transistor logic mux in a hierarchical tree structure. This structure will have the inputs to the mux driving the source-drain of the transistors with the select lines of the mux driving the gates. The select lines (gates) will be separate voltages sources than the inputs allowing for dual Vdd operation and analysis.

The final topology we will analyze is a driven inverted tree or PTL stack as mentioned above in the related work [4]. This topology will need to be modified to work in sub threshold and with dual V_{DD} operation. Furthermore, we will modify it in order to reduce its transistor count by removing the SB network and pre-charging the S network.

Research

The novelty of this research is the application of dual-V_{DD} for driving the gates of PTL at a higher voltage than the source-drain input voltage of the PTL. The comparison of different PTL topologies for LUT implementation will be a secondary focus of this project. Additionally, for this project, some novelty comes from the modification and analysis of the PTL stack structure in sub-threshold, and dual-V_{DD} operation.

Simulation

In all three topologies, the transmission gate mux, PTL mux, and stack PTL, the main simulation we will look at is energy versus delay. These energy – delay graphs will be generated by separating the circuits into dual-V_{DD} operation with separate input voltages (V_{DD}) and gate voltages (Vg). Then to make the energy-delay graphs we will perform parametric sweeps, sweeping both V_{DD} and Vg. Finally, we also plan on graphing leakage current versus V_{DD} for all three topologies.

Expected Outcomes

Using the three aforementioned topologies, we expect that by using dual-V_{DD} operation, we will get improved energy-delay curves for all of the topologies when Vg is higher than V_{DD}. We expect that initially the transmission gate topology will have a better delay metric when V_{DD} is equal to Vg. However, when Vg is significantly higher than V_{DD}, we expect the PTL mux and PTL stack to be full swing again with improved delay characteristics. With delay being similar, we expect PTL stack to have better energy performance because of reduced leakage paths. Also, other metrics such as size must be taken into consideration when considering tradeoffs for the topologies. For size, we expect the PTL mux to be the smallest due to the fact that it has fewer transistors than the PTL stack and many fewer PMOS transistors than the transmission gate topology.

Preliminary Work

To examine the concept of applying dual-V_{DD} supply to a PTL network, we have tested the operation of a 16-to-1 PTL mux. Fig. 2 shows a simple 2T 2-to-1 mux, while Fig. 3 shows a 30T 16-to-1 mux composed of the 2-to-1 muxes.

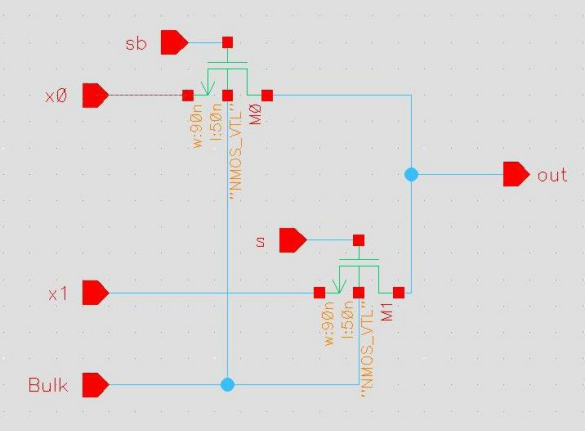

Figure 2. A single PTL 2-to-1 mux.

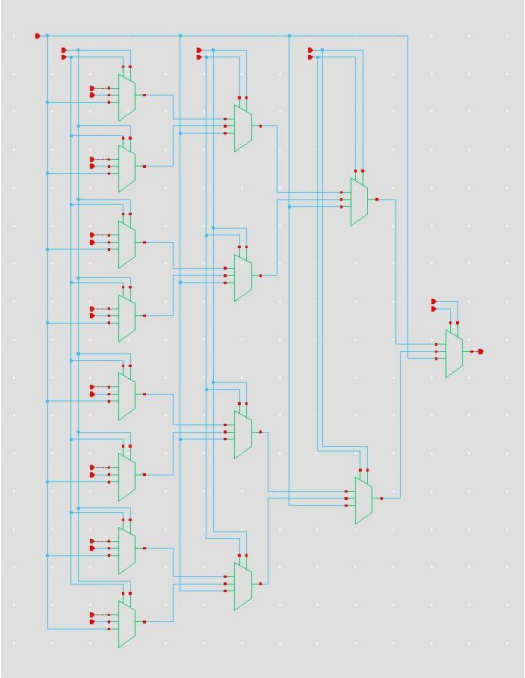

Figure 3. A 16-to-1 PTL mux.

A transient analysis with parametric sweep of the low-V_{DD} (i.e., the one associated with the 16 source-drain inputs) multiple times, holding the high V_{DD} (i.e., that driving the select lines or gate terminals) constant at a different value for each simulation. Some of the energy-delay curves are shown in Fig. 4 below (note: subsequent work will swap the E-D axes). For each Vg (that is, the high V_{DD} level), there is an optimum low-V_{DD} for minimizing energy and delay. Fig. 5 illustrates a transient plot of the input and output voltages for the mux for varying low V_{DD} with the high V_{DD} fixed at 1.1V. As the lower supply approaches a V_t drop of the high supply, the swing saturates and results in a prolonged rise time, but when they are sufficiently separated, the delay of the mux is very small, with the rise time of the driving inverter being a more important factor.

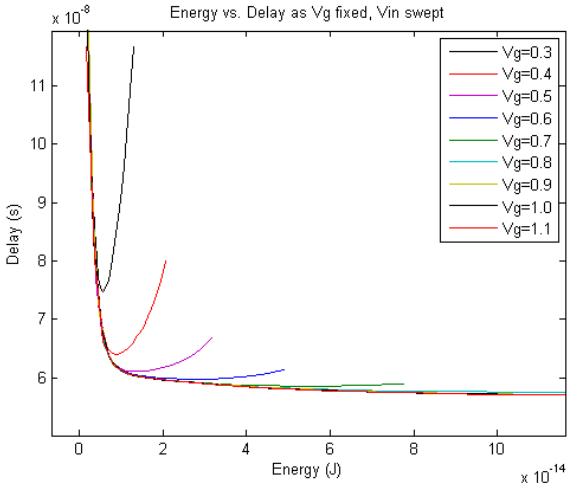

Figure 4. Energy-delay curves as the low V_{DD} supply is swept, for various high-V_{DD} values.

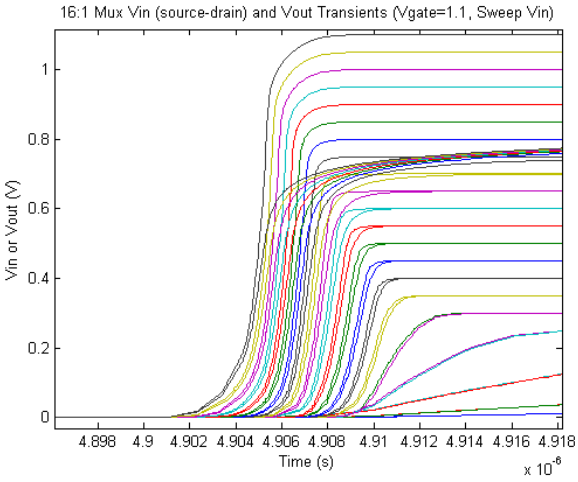

Figure 5. Transient plot of the input and output signals of the 16-to-1 mux for varying low-V_{DD}.

Schedule and Division of Work

Week	Task(s) Scheduled	Assigned
Oct. 14, 2010	Develop project idea from design review 1 work. Submit project proposal.	Jeff and Sam
Oct. 21, 2010	Construct dual-V_{DD} transmission gate mux-based LUT (base case) and corresponding test bench circuits in Cadence schematic editor.	Jeff
	Construct dual-V_{DD} PTL mux-based LUT and test bench.	Sam
Oct. 28, 2010	Simulate TX gate and PTL based LUTs in sub-V_t with varying high and low V_{DD} differences using (hopefully) OCEAN scripting.	Sam and Jeff
	Write MATLAB scripts (as necessary) to process and plot E-D results from the simulations.	Jeff
Nov. 4, 2010	Compile to-date results and prepare Design Review 2 for submission.	Jeff and Sam
	Begin constructing stack-based LUT circuit.	Jeff and Sam
Nov. 11, 2010	Complete construction of stack-based LUT and test bench circuits.	Sam
	Simulate stack-based LUT with sub-V_t and varying dual-V_{DD} levels.	Jeff
Nov. 18, 2010	Modify stack-based LUT for lower transistor count.	Jeff
	Repeat simulations with lower-count stack-based LUT.	Sam
Nov. 25, 2010	Write final report and presentation slides leading into holiday.	Jeff and Sam
Dec. 2, 2010	Complete and submit final report and presentation.	Jeff and Sam

References

[1] F. Li, Y. Lin, L. He, and J. Cong, "Low-power FPGA using pre-defined dual-Vdd/dual-Vt fabrics," in *Proc. 12th Int. Symp. Field Programmable Gate Arrays*, Monterey, CA, 2004, pp. 42-50.

[2] A. Gayasen, K. Lee, N. Vijaykrishnan, M.J. Irwin, and T. Tuan, "A dual-VDD low power FPGA architecture," in *Proc. Int. Conf. Field Programmable Logic and Applications*, Antwerp, Belgium, 2004, pp. 145-157.

[3] J.F. Ryan, B.H. Calhoun, "A sub-threshold FPGA with low-swing dual-V_{DD} interconnect in 90nm CMOS," in *IEEE Custom Integrated Circuits Conference*, San Jose, CA, 2010.

[4] L.P. Alarcón, T.-T. Liu, M.D. Pierson, and J.M. Rabaey, "Exploring very low-energy logic: a case study," in J. Low Power Electronics, vol. 3, no. 3, pp. 223-233, 2007.